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TITLE: REFRESH CIRCUIT FOR DRAM

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ABSTRACT:

PURPOSE: To decrease the number of times for executing a refresh cycle and to improve the throughput of access by preventing a refresh operation from being executed to the same row address as a cell selected by a memory access operation.

CONSTITUTION: Based on a clock signal CLK, a refresh (RF) interval timer circuit 6 measures the interval of the RF operation execution and outputs the RF request of the correspondent address and an RF order circuit 7 determines the execution order, demands the output of the RF address to an address circuit 8 and demands the execution of the RF cycle at a DRAM to an RF timing control circuit 10. The circuit 8 outputs RF address outputs RA<SB>0</SB>-RA<SB>7</SB> to an address switching circuit 9. While receiving RF address signals MA<SB>0</SB>-MA<SB>8</SB> from the circuit 9 and the inverse of RAS and CAS signals from a DRAM access control circuit 4, the circuit 10 successively refreshes respective rows excepting for the same row as the cell accessed at the time of the preceding access at timing for the inverse of RAS only refresh cycle when the inverse of CAS is made H.